AMENDMENTS TO THE CLAIMS

Claims 1-26. (Cancelled)

27. (Original) A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and processor comprising a transistor, said transistor comprising:

source and drain regions provided on a SOI substrate, said source and drain regions being of a first conductivity type; and

a gate stack fabricated on said SOI substrate, said gate stack including a conductive layer of a second conductivity type.

28. (Original) The processor-based system of claim 27, wherein said transistor is a fully-depleted SOI transistor.

29. (Original) The processor-based system of claim 28, wherein said fully-depleted SOI transistor is a fully-depleted SOI NMOS transistor.

30. (Original) The processor-based system of claim 27, wherein said first conductivity type is n-type and said second conductivity type is p-type.

31. (Original) The processor-based system of claim 27, wherein said first conductivity type is p-type and said second conductivity type is n-type.

32. (Original) The processor-based system of claim 27, wherein said conductive layer is a doped polysilicon layer.

33. (Original) The processor-based system of claim 27, wherein said conductive layer is a doped silicon/germanium layer.

34. (Original) The processor-based system of claim 27, wherein said gate structure further comprises a silicide layer over said conductive layer.

35. (Original) The processor-based system of claim 27, wherein said gate structure further comprises a cap layer over said conductive layer.

Claims 36-86. (Cancelled)